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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	4

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,510	ANG, BOON SEONG	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 23-25* is/are pending in the application.

4a) Of the above claim(s) *21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant is required to cancel the non-elected claims 21 and 22.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the programmable logic device and field programmable gate array in the claims 15-16 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 1 recites the limitation "a circuit arrangement" and "a first circuit arrangement" in preamble. It is recommended to use "a first circuit arrangement" and "a second circuit arrangement" to avoid any confusion between these two circuit arrangements.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a programmable device" on line 9. There is sufficient antecedent basis for this limitation in the claim. Claims 2-20 are rejected because they incorporate claim 1's limitations.

Claims 15 and 16 recite the limitations of "the programmable device". It is not clear which programmable device of claim 1 that claims 15 and 16 are referring to.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-14, 18-20, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi et al. (U.S. Patent No. 6,708,069) in view of the admitted prior art.

Referring to claim 1: Ohashi discloses a circuit arrangement (structure 205 in figures 2 and 3) for interfacing a first circuit arrangement (structures 201, 202, 203, and 204 in figure 2) with a bus functioning in accordance with a bus protocol, comprising a bus interface circuit (figure 3, where the structure 205 interface with structures 206 and 100) having a port arranged to be coupled to the bus, a bus processing block (figure 3, structures 304, 3031, 3032, 3033, 3021, 3022, and 3023) coupled to the bus interface circuit, the bus processing block implemented with a programmable device (figure 3, structure 304) and configured to perform selected processing in response to selected bus messages; and a filter circuit (the means to compare the message as stated in column 7, last line, column 8, lines 1-4, comparing the message-sending condition-identifying portions) coupled to the bus interface circuit and to the bus processing block, the filter circuit implemented with a programmable device (column 7, last line, column 8, lines 1-4, comparing the message-sending condition-identifying portions) and configured to direct bus messages to a selected one of the bus interface circuit and the bus process (either go through or bypass the control parts, structures 304, 3031, 3032, 3033, 3021, 3022, and 3023).

Although Ohashi does not disclose separate physical structures for the bus interface circuit and filter circuit, both MPEP and court have held that forming in one piece an article which has formerly been formed in two pieces and put together, and constructing a formerly integral structure in various elements involve only routine skill in the art (MPEP 2144, Howard v. Detroit Stove Works, 150 U.S. 164, Nerwin v. Erlichman, 168 USPQ 177, 179).

Ohashi does not explicitly disclose the physical and link layers. The disclosed prior art (Application, page 2) discloses that the physical and link layers are known to the bus communication. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teaching of physical, link layers, and separating a formerly integral structure to Ohashi because the physical and link layers are the fundamental practice for the bus communication, and the MPEP and court have held that constructing a formerly integral structure in various elements involve only routine skill in the art.

Referring to claim 2: Ohashi discloses that the filter circuit is configured to direct bus messages to a selected one of the bus interface circuit and the bus processing block in response to at least one of a bus operation code, an address, and initiator identification code in each of the bus messages (column 7, last line, column 8, lines 1-4).

Referring to claim 3: As stated in the claim 1's argument, Ohashi discloses a filter circuit coupled to the bus interface circuit and to the bus processing block, but Ohashi's does not explicit disclose the filter circuit receives messages from the first circuit arrangement. Ohashi discloses that the filter circuit receives the messages from the exterior bus (figure 3, structure 100). Although Ohashi does not explicitly disclose an interior filter circuit, both MPEP and court have held that rearrangement of parts and duplication of parts only involve routine skill in

the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8, In re Japikse, 86 USPQ 70). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention because it only involves routine skill in the art to duplicate the Ohashi's filter circuit for both interior bus and exterior bus or arrange Ohashi's filter circuit from exterior bus to interior bus.

Referring to claim 5: Ohashi does not explicitly disclose a cache and a translation look-aside buffer (TLB) that maps virtual addresses to physical addresses of data stored in the cache, the TLB further including a flag with a selected value for selected areas of memory, and the interior filter circuit is coupled to the TLB and further configured to directed selected bus messages to the bus processing block responsive to the value of the flag in the TLB. The prior art (Application, page 2) discloses that it is known that the semantics layer observes the transmitting operations and forwards information to the blocks in the cache.

Referring to claim 7: Ohashi discloses the CAM (figure 3, structures 301 and 305) and values representing selected address range (figure 3, structures 3021, 3022, and 3023), and Ohashi discloses comparing the address of the message (column 4, lines 35-50).

Referring to claim 8: Claim 7's argument applies, furthermore, the prior art discloses that it is known to select messages based on the operation types (Application, page 2).

Referring to claim 9: Ohashi discloses the CAM (figure 3, structures 301 and 305) and values representing selected address range (figure 3, structures 3021, 3022, and 3023), and Ohashi discloses comparing the address of the message (column 4, lines 35-50). Furthermore, the prior art discloses that it is known to select messages based on the operation types (Application, page 2).

Referring to claims 10-11: As stated in the claim 1's argument, Ohashi discloses a filter circuit coupled to the bus interface circuit and to the bus processing block, and the filter circuit receives messages from the exterior bus (figure 3, structure 100).

Referring to claim 12: Ohashi discloses the CAM (figure 3, structures 301 and 305) and values representing selected address range (figure 3, structures 3021, 3022, and 3023), and Ohashi discloses comparing the address of the message (column 4, lines 35-50).

Referring to claim 13: Claim 7's argument applies, furthermore, the prior art discloses that it is known to select messages based on the operation types (Application, page 2).

Referring to claim 14: Ohashi discloses the CAM (figure 3, structures 301 and 305) and values representing selected address range (figure 3, structures 3021, 3022, and 3023), and Ohashi discloses comparing the address of the message (column 4, lines 35-50). Furthermore, the prior art discloses that it is known to select messages based on the operation types (Application, page 2).

Referring to claim 18: Ohashi's processing block is configured to receive bus messages from the bus without interruption of the first circuit arrangement (figures 2-3).

Referring to claim 19: Ohashi discloses the RAM (figure 2, structure 203) but not within the processing block. Ohashi discloses memory (figure 3, structures 301 and 305) coupled to the bus-processing block, which is the RAM.

Referring to claim 20: Ohashi's circuit transmits the message to the bus (figure 3 structure 206), thus, it initiates transmission of bus message over the bus via the bus interface circuit.

Referring to claim 23: Ohashi discloses a circuit arrangement (structure 205 in figures 2 and 3) for interfacing a first circuit arrangement (structures 201, 202, 203, and 204 in figure 2)

with a bus functioning in accordance with a bus protocol, comprising a bus interface circuit (figure 3, where the structure 205 interface with structures 206 and 100) having a port arranged to be coupled to the bus, a bus processing block (figure 3, structures 304, 3031, 3032, 3033, 3021, 3022, and 3023) coupled to the bus interface circuit, the bus processing block implemented with a programmable device (figure 3, structure 304) and configured to perform selected processing in response to selected bus messages; and a filter circuit (the means to compare the message as stated in column 7, last line, column 8, lines 1-4, comparing the message-sending condition-identifying portions) coupled to the bus interface circuit and to the bus processing block, the filter circuit implemented with a programmable device (column 7, last line, column 8, lines 1-4, comparing the message-sending condition-identifying portions) and configured to direct bus messages to a selected one of the bus interface circuit and the bus process (either go through or bypass the control parts, structures 304, 3031, 3032, 3033, 3021, 3022, and 3023), which is the first class and the second class of bus messages.

Although Ohashi does not disclose separate physical structures for the bus interface circuit and filter circuit, both MPEP and court have held that forming in one piece an article which has formerly been formed in two pieces and put together, and constructing a formerly integral structure in various elements involve only routine skill in the art (MPEP 2144, Howard v. Detroit Stove Works, 150 U.S. 164, Nerwin v. Erlichman, 168 USPQ 177, 179).
Ohashi discloses a filter circuit coupled to the bus interface circuit and to the bus processing block, but Ohashi's does not explicit disclose the filter circuit receives messages from the first circuit arrangement.

Ohashi discloses that the filter circuit receives the messages from the exterior bus (figure 3, structure 100). Although Ohashi does not explicitly disclose an interior filter circuit, both MPEP and court have held that rearrangement of parts and duplication of parts only involve routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8, In re Japikse, 86 USPQ 70). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention because it only involves routine skill in the art to duplicate the Ohashi's filter circuit for both interior bus and exterior bus or arrange Ohashi's filter circuit from exterior bus to interior bus.

Ohashi does not explicitly disclose the physical and link layers. The disclosed prior art discloses that the physical and link layers are known to the bus communication. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teaching of physical, link layers, and separating a formerly integral structure to Ohashi because the physical and link layers are the fundamental practice for the bus communication, and the MPEP and court have held that constructing a formerly integral structure in various elements involve only routine skill in the art.

Referring to claim 24: Ohashi discloses a programmable filter (the means to compare the message as stated in column 7, last line, column 8, lines 1-4, comparing the message-sending condition-identifying portions).

Referring to claim 25: Ohashi discloses a circuit arrangement (structure 205 in figures 2 and 3) for interfacing a first circuit arrangement (structures 201, 202, 203, and 204 in figure 2) with a bus functioning in accordance with a bus protocol, comprising a bus interface circuit (figure 3, where the structure 205 interface with structures 206 and 100) having a port arranged

to be coupled to the bus, a bus processing block (figure 3, structures 304, 3031, 3032, 3033, 3021, 3022, and 3023) coupled to the bus interface circuit, the bus processing block implemented with a programmable device (figure 3, structure 304) and configured to perform selected processing in response to selected bus messages; and a filter circuit (the means to compare the message as stated in column 7, last line, column 8, lines 1-4, comparing the message-sending condition-identifying portions) coupled to the bus interface circuit and to the bus processing block, the filter circuit implemented with a programmable device (column 7, last line, column 8, lines 1-4, comparing the message-sending condition-identifying portions) and configured to direct bus messages to a selected one of the bus interface circuit and the bus process (either go through or bypass the control parts, structures 304, 3031, 3032, 3033, 3021, 3022, and 3023), which is the first class and the second class of bus messages.

Although Ohashi does not disclose separate physical structures for the bus interface circuit and filter circuit, both MPEP and court have held that forming in one piece an article which has formerly been formed in two pieces and put together, and constructing a formerly integral structure in various elements involve only routine skill in the art (MPEP 2144, Howard v. Detroit Stove Works, 150 U.S. 164, Nerwin v. Erlichman, 168 USPQ 177, 179). Ohashi discloses a filter circuit coupled to the bus interface circuit and to the bus processing block, but Ohashi's does not explicit disclose the filter circuit receives messages from the first circuit arrangement.

Ohashi discloses that the filter circuit receives the messages from the exterior bus (figure 3, structure 100). Although Ohashi does not explicitly disclose an interior filter circuit, both MPEP and court have held that rearrangement of parts and duplication of parts only involve

routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8, In re Japikse, 86 USPQ 70). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention because it only involves routine skill in the art to duplicate the Ohashi's filter circuit for both interior bus and exterior bus or arrange Ohashi's filter circuit from exterior bus to interior bus.

Ohashi does not explicitly disclose the physical and link layers. The disclosed prior art discloses that the physical and link layers are known to the bus communication. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teaching of physical, link layers, and separating a formerly integral structure to Ohashi because the physical and link layers are the fundamental practice for the bus communication, and the MPEP and court have held that constructing a formerly integral structure in various elements involve only routine skill in the art.

9. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi view of the admitted prior art, and in further view of Kelly (U.S. Patent No. 5,734,872).

Referring to claims 15-16: Ohashi does not explicitly disclose a field programmable gate array. Kelly discloses that the field programmable gate array is a common practice in the computer field to interconnect CPU (figure 1). Thus, it would have been obvious to one having ordinary skill in the computer art to adapt Kelly's teaching to Ohashi because Kelly teaches one to improve the performance by employing FPGA to perform any pre-processing for the CPU.

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi view of the admitted prior art, and in further view of Kardach et al. (U.S. Patent No. 5,560,001).

Referring to claim 17: Ohashi does not disclose a microcode engine. Kardach teaches that it is known to employ a microcode engine to respond to an external request and to execute a sequence of steps. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Kardach's teaching to Ohashi because Kardach teaches one to improve the performance by employing a microcode engine to perform any pre-processing for the CPU.

Allowable Subject Matter

11. Claims 4 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior arts on record do not disclose or teach the notification data provided to the bus processing block.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 703-305-4571. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-308-3110. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin King
June 17, 2004

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TC2100